CLAIMS

What is claimed is:

1. A circuit for equalizing a signal comprising;

feed-forward equalizer (FFE) for receiving an input signal providing a partially equalized signal;

a slicer for receiving the partially equalized signal for providing decoded bit values for the partially equalized signal;

a signal quality circuit for measuring the error in the signal from the FFE and providing an error output; and

a convergence algorithm circuit for receiving the error output and controlling the FFE and the DFE, wherein an optimum equalized signal is provided and the recovered clock signal is independent of the equalization.

2. The method of claim 1 wherein the feed-forward equalizer (FFE) comprises a fractionally spaced transversal filter that randomly samples error values and converges the filter without requiring the tap values.